ACH1190 Audio Host Processor

Features

- 60-pin lead-free/RoHS compliant
- QFN or BGA package
- ARM Cortex-M4 with floating point processing option
- Two programmable fractional-N synthesizers to reduce interference
  - Supplies CPU clock frequencies, up to max 240MHz
  - Supplies integrated audio codec
- 960k byte internal SRAM
- SPI serial flash interface
- Support sleep and deep sleep mode for low power consumption
- Integrated high-fidelity stereo audio codec
  - Supports Line-in/out and mic-in/headset out
  - Differential mic input
  - 96dB SNR audio output
  - Optional digital interface (I^2S)
- Multiple external interfaces to adapt to various IoT and applications needs
  - 2 x UART
  - I^2C
  - 1 x 10-bit ADCs
  - SPI
  - 11 x GPIO
- Clocks
  - Reference clock input 26MHz
  - Low power clock input at 32.768 kHz
  - 2 x clock outputs
- Timers
  - 8 x 32-bit high speed timers
  - 4 timers with independent interrupts

Description

The ACH1190 is a single-chip host processor solution that is fully optimized for Audio and IoT applications. Built with ARM Cortex-M4, floating point, this host processor runs up to 240MHz (300 DMIPS) and is ideal for audio and video processing. It integrates 960K bytes of embedded SRAM for code and data execution. It also integrates a high-fidelity, 96dB SNR stereo audio codec for audio applications, with two fractional-N synthesizers to provide separate clock frequencies to CPU and audio codec to reduce audio interference. Equipped with various external interfaces, ACH1190 can be designed in numerous types of host application scenarios. The ACH1190 also supports a crystal driver interface, thus able to generate reference clocks to various wireless connectivity radio controllers, such as Wifi/Bluetooth/Zigbee.

With CSP and QFN package options, it supports a high level of integration, compact and cost-effective designs, and delivers fast time-to-market.

Contents

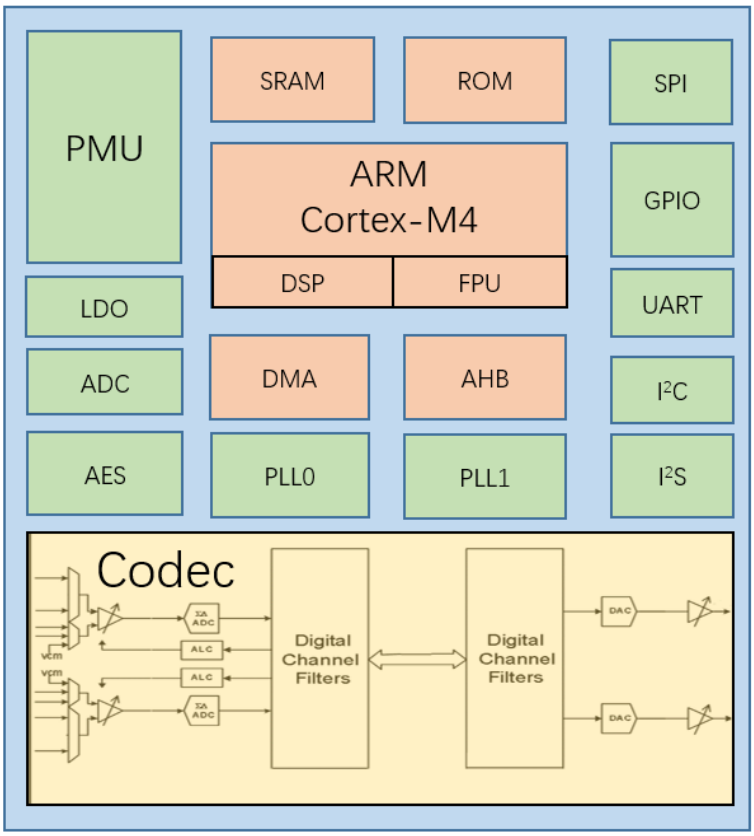
1. Introduction

The ACH1190 is a host processor single-chip solution, fully optimized for audio DSP and wireless host embedded applications featuring an ARM Cortex-M4 floating point processor. Integrating a high-fidelity stereo audio codec, it can support differential microphone inputs, headphone output, and Line-in/out. It also includes two fractional-N PLL blocks providing different high accuracy clocks, for the main CPU and audio codec – significantly reducing interference. The main CPU system can run up to 240MHz for intensive audio/video applications, audio DSP processing, and general-purpose application hosting. The ACH1190 also comes with 960K byte internal run-time SRAM. With a variety of external interfaces, UART, SPI, I²C, I²S, ADCs, and GPIOs, it can be easily support designs for most applications with lower BOM and external component cost.

2. General Hardware Description

2.1. Block Diagram

Figure 1. ACH1190 internal block diagram



2.2. Pin functions

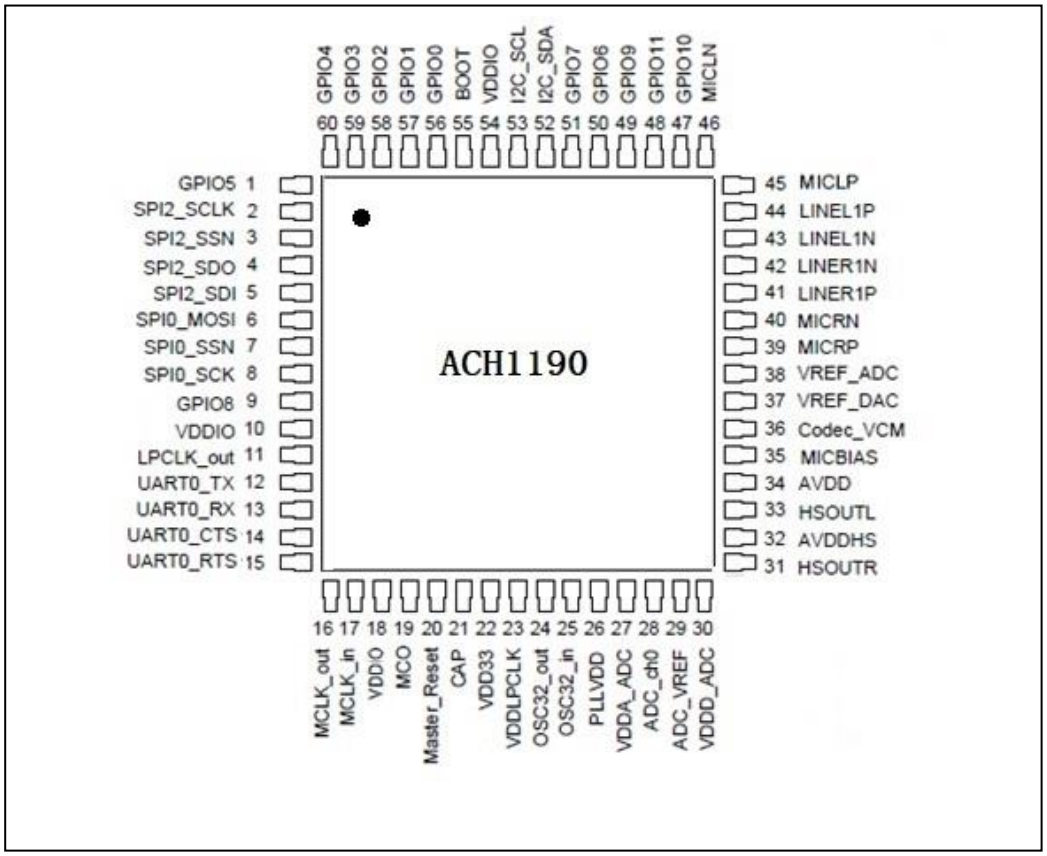
Table 1. ACH1190 functional and supply pin list QFN package

Pad	Name (Default)	Alternate usage ALT_0	Alternate usage ALT_1	Description
	Digital Signal			
6	SPI0_MOSI	UART1_CTS		RF Controller Interface
7	SPI0_NSS	UART1_RTS		
8	SPI0_SCK	UART1_TX		
9	SPI0_MISO	UART1_RX	GPIO_8	
12	UART0_TX			UART0
13	UART0_RX			
14	UART0_CTS			
15	UART0_RTS			
47	JTDI	UART2_RX	GPIO_10	JTAG
48	JTDO	UART2_TX	GPIO_11	
49	TRSTn	UART2_CTS	GPIO_9	
56	GPIO_0	UART2_RTS		
57	GPIO_1	I2S0_WS	SPI1_CS	GPIO
58	GPIO_2	I2S0_CK	SPI1_CLK	
59	GPIO_3	I2S0_RX	SPI1_MISO	
60	GPIO_4	I2S0_TX	SPI1_MOSI	
1	GPIO_5			
2	SPI2 SCK			SPI2 Serial NOR Flash
3	SPI2 SS			
4	SPI2 SDO			
5	SPI2 SDI			
50	TCK/SWCLK	GPIO_6		JTAG or User Interface
51	TMS/SWDIO	GPIO_7		
52	I2C0_SDA			I2C0
53	I2C0_SCL			
	Clock Signal			
24	OSC32_OUT			32kHz crystal input (differential pair)
25	OSC32_IN			32kHz crystal input
16	OSC_OUT			26MHz crystal input (differential pair)
17	OSC_IN			26MHz crystal input
19	MCO			Main Clock output (26MHz default)
11	LPCLK_OUT			32kHz buffer clock output (LPO default)
	Audio Signal			
45	MICIP_L			Microphone Input
46	MICIN_L			
39	MICIP_R			

40	MICIN_R			
44	LINE_L_1P			Line-In
43	LINE_L_1N			
42	LINE_R_1N			
41	LINE_R_1P			
31	RHPOUT			Headset Output (8 ohms)
33	LHPOUT			
	Control Signal			
20	RESET			Reset (Active Low)
55	BOOT			Test pin
	Analog Signal			
28	ADC0			10-bit ADC
	Reference Signal			
21	Vcap			
29	Vref_ADC			
38	Vref_AD			Codec Internally generated ADCs reference voltage pin for off-chip decoupling. Connect 1uF tantalum and 100nF ceramic capacitors to agndref.
37	Vref_DA			Codec Internally generated DACs reference voltage pin for off-chip decoupling. Connect 1uF tantalum and 100nF ceramic capacitors to agndref.
36	Codec_VCM			Codec Internally generated common-mode voltage pin for off-chip decoupling. Connect 10uF tantalum and 100nF ceramic capacitors to agnd.
35	MICBIAS			Microphone bias voltage output
	Power Supply			
30	VDDD_ADC			ADC Analog Supply
27	VDDA_ADC			ADC Digital Supply
32	AVDDHS			Codec Analog power supply for headset drivers. Connect 10uF tantalum and 100nF ceramic capacitors to AGND.
34	AVDD			Codec Analog power supply. Connect 10uF tantalum and 100nF ceramic capacitors to AGND.
26	PLLVDD			PLL Analog Supply
23	VDDLPCLK			PLL IO Supply
22	VDD33			Power supply (3.3V)
10	VDDIO			Digital IO Supply
18	VDDIO			
54	VDDIO			
	PAD			GND

2.3. Pinout Diagram

Figure 2. ACH1190 QFN60 pinout



3. Reset

3.1. Boot modes

An embedded BOOT ROM will run at startup.

When the BOOT PIN is low (0), the SPI 2 is used to load an 8K byte section of an external Flash memory into the internal RAM: loads 8K bytes from location 0x00000000 external Flash to location 0x20000000 internal RAM.

When the BOOT PIN is high (1), the UART 0 boot mode interface will become active. This interface allows data to be loaded from UART 0 into RAM using a set of boot commands. Note that these boot commands are generally used for testing and are not included in this document.

4. System Memory Map

Address	Feature
0x0000_0000 to 0x000F_FFFF	BOOT ROM
0x2000_0000 to 0x200F_EFFF	SRAM
0x4002 1800 – 0x4002 1FFF	SPI0
0x4002 2000 – 0x4002 27FF	SPI1
0x4002 2800 – 0x4002 2FFF	I2S0
0x4002 3000 – 0x4002 37FF	UART0
0x4002 3800 – 0x4002 3FFF	UART1
0x4002 4000 – 0x4002 47FF	I2S1 CODEC
0x4002 4800 – 0x4002 4FFF	SPI2 FLASH
0x4002 5000 – 0x4002 57FF	I2C0
0x4002 5800 – 0x4002 5FFF	CODEC
0x4002 6000 – 0x4002 67FF	UART2
0x4003 1800 – 0x4003 1FFF	GPIO
0x4003 3000 – 0x4003 37FF	WDT
0x4003 3800 – 0x4003 3FFF	ADC0
0x4003 4000 – 0x4003 47FF	ADC1
0x4003 4800 – 0x4003 4FFF	AES
0x4003 5800 – 0x4003 5FFF	SYSCFG
0x4003 6000 – 0x4003 67FF	TIMER

5. System Control Block register, SCB

The ARM Cortex M4 system control block register map is presented below. For further details on this register and other ARM core items, see the ARM help center at: http://infocenter.arm.com/help/topic/com.arm.doc.dui0553b/DUI0553.pdf

Address	Name	Type	Reset value	Description
0xE000E008	ACTLR	RW	0x00000000	Auxiliary Control Register
0xE000ED00	CPUID	RO	0x410FC240	CPUID Base Register
0xE000ED04	ICSR	RW	0x00000000	Interrupt Control and State Register
0xE000ED08	VTOR	RW	0x00000000	Vector Table Offset Register
0xE000ED0C	AIRCR	RW	0xFA050000	Application Interrupt and Reset Control Register
0xE000ED10	SCR	RW	0x00000000	System Control Register
0xE000ED14	CCR	RW	0x00000020	Configuration and Control Register
0xE000ED18	SHPR1	RW	0x00000000	System Handler Priority Register 1
0xE000ED1C	SHPR2	RW	0x00000000	System Handler Priority Register 2
0xE000ED20	SHPR3	RW	0x00000000	System Handler Priority Register 3
0xE000ED24	SHCRS	RW	0x00000000	System Handler Control and State Register
0xE000ED28	CFSR	RW	0x00000000	Configurable Fault Status Register
0xE000ED28	MMSR[1]	RW	0x00	MemManage Fault Status Register
0xE000ED29	BFSR[1]	RW	0x00	BusFault Status Register
0xE000ED2A	UFSR[1]	RW	0x0000	UsageFault Status Register
0xE000ED2C	HFSR	RW	0x00000000	HardFault Status Register
0xE000ED34	MMAR	RW	NA	MemManage Fault Address Register
0xE000ED38	BFAR	RW	NA	BusFault Address Register
0xE000ED3C	AFSR	RW	0x00000000	Auxiliary Fault Status Register

1. A subregister of the CFSR.

6. Alternative MUX Control

Many of the I/O lines have alternative functions. Use the output enable reg0 and reg1 to control these settings.
SYSCFG register
CFG26, offset 0x6C
CFG27, offset 0x70

0x6C	sys_cfg_reg26, output_enable_reg0	Default value
1:0	00, select SPI0_MOSI as output 01,10,11 select UART1_CTS as input	0
3:2	01 ,select UART1_RTS as output 00,10,11 select SPI0_NSS as output	0
5:4	01, select UART1_TX as output 00,10,11 select SPI0_SCK as output	0
7:6	10, select GPIO_8 00,01,11 select SPI0_SDI and UART1_RX as input	0
15:8	Reserved	0
17:16	10, select GPIO_10 00,01,11 select JTDI, UART2_RX	0
19:18	00, select JTDO as output 01, select UART2_TX as output 10, select GPIO_11	0
21:20	10, select GPIO_9 00,01,11 select TRSTn, UART2_CTS	0
23:22	00, select GPIO_0 01, select UART2_RTS as output	0
25:24	00, select GPIO_1 01, select I2S0_WS as output 10, select SPI1_CS as output 11, Reserved	0
27:26	00, select GPIO_2 01, select I2S0_CK_sel_stage1 as output 10, select SPI1_CLK as output 11, Reserved	0
29:28	00, select GPIO_3 01,10 select SPI1_MISO 11, I2S0_RX as output	0
31:30	00, select GPIO_4 01, select I2S0_TX as output 10, select SPI1_MOSI as output 11, Reserved	0

0x70	sys_cfg_reg27, output_enable_reg1	Select
1:0	00, select GPIO_5 01,10,11 Reserved	0
15:14	00, select TCK/SWCLK 01,10,11 select GPIO_6	0
17:16	00, select SWDIO/TMS as output 01, select GPIO_7 10,11 select SWDIO/TMS as input	0
19:18	00, select I2C0_SDA 01,10,11 Reserved	0

21:20	00, select I2C0_SCL 01,10,11 Reserved	0
31:22	Reserved	

7. Serial Peripheral Interface, SPI

Three SPI ports are supported, usable in Master mode up to 40Mbps. Below is the feature list for the SPI devices:

- Data bus widths of 8, 16, and 32 bits.
- FIFO depth – Configurable depth of the transmit and receive FIFO buffers from 1 to 128 words deep.
- Programmable levels of FIFO interrupt for receive and transmit.
- Independent masking of interrupts – Master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow interrupts can all be masked independently.
- Multi-master contention detection – Informs the processor of multiple serial-master accesses on the serial bus.
- Programmable delay on the sample time of the received serial data bit (rxd), when configured in Master Mode; enables programmable control of routing delays resulting in higher serial data-bit rates.
- Serial interface operation – Choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire.
- Clock bit-rate – Dynamic control of the serial bit rate of the data transfer.
- Hardware/software slave-select – Dedicated hardware slave-select lines can be used or software control can be used to target the serial-slave device.
- Serial clock polarity – This configuration option selects the serial-clock polarity of the SPI format directly after reset.
- Serial clock phase – This configuration option selects the serial-clock phase of the SPI format directly after reset.

7.1. SPI Register Definitions

Register	Offset	Size	Description
CTRLR0	0x00	21b	Control Register 0
CTRLR1	0x04	16b	Control Register 1
SSIENR	0x08	1b	SSI Enable
BAUDR	0x14	16b	Baud Rate Select
TXFTLR	0x18	6b	Transmit FIFO Threshold Level
RXFTLR	0x1C	6b	Receive FIFO Threshold Level
TXFLR	0x20	7b	Transmit FIFO Level
RXFLR	0x24	7b	Receive FIFO Level
SR	0x28	7b	Status
IMR	0x2C	6b	Interrupt Mask
ISR	0x30	6b	Interrupt Status
RISR	0x34	6b	Raw Interrupt Status
TXOICR	0x38	1b	Transmit FIFO Overflow Interrupt Clear
RXOCR	0x3C	1b	Receive FIFO Overflow Interrupt Clear
RXUICR	0x40	1b	Receive FIFO Underflow Interrupt Clear
MSTICR	0x44	1b	Multi-Master Interrupt Clear
ICR	0x48	1b	Interrupt Clear
DR	0x60	32b	Data

7.1.1 CTRLR0

Setting	Position	Description
DFS	0-3	Selects frame size in 16bit xfer mode. Data must be Right justified. Use: binary value +1. For example

		0x4 = 5-bit size, 0xF = 16-bit size.
FRF	4-5	Frame format. 00: Motorola SPI, 01: Texas Instruments SSP, 10 and 11: reserved.
SCPH	6	Clock phase, valid in Motorola SPI mode. 0: middle of first bit, 1: start of first bit.
SCPOL	7	Clock polarity, valid in Motorola SPI mode. 0: inactive low, 1: inactive high
Reserved	8-15	
DFS_32	16-20	Selects frame size in 32bit xfer mode. Data must be right justified. Use binary value +1. For example 0x1F = 32-bit size.
Reserved	21-31	

7.1.2 CTRLR1

Setting	Position	Description
NDF	0-15	Number of data frames. Receive data until the number of frames equals value +1. Maximum of 64KB data.

7.1.3 SSIENR

Setting	Position	Description
SSI_EN	0	When disable, all transfers are halted, transmit and receive FIFO buffers are cleared. Maybe be disabled for low power mode. 1: enable, 0: disable.

7.1.4 BAUDR

Setting	Position	Description
SCKDV	0-15	The frequency of the sclk is Fsclk = Fssi_clk/SCKDV

7.1.5 TXFTLR

Setting	Position	Description
TFT	0-6	Transmit FIFO Threshold. Level of entries, TFT value, (or below) at which the transmit FIFO controller triggers the tx empty interrupt: 0-127. For example: 0x0F will assert TXE when 15 or fewer data entries are present.

7.1.6 RXFTLR

Setting	Position	Description
RFT	0-6	Receive FIFO Threshold. Level of entries, RFT value +1, (or above) at which the receive FIFO controller triggers the RX full interrupt: 1-128. For example: 0x7F will assert RXF when 256 or more data entries are present.

7.1.7 TXFLR

Setting	Position	Description
TXTFL	0-7	Transmit FIFO Level. Number of data entries in the transmit FIFO, 0-128.

7.1.8 RXFLR

Setting	Position	Description
RFTFL	0-7	Receive FIFO Level. Number of data entries in the transmit FIFO, 0-128.

7.1.9 SR

Setting	Position	Description
Busy	0	SSI Busy Flag. When set, indicates that a transfer is in progress. When clear, indicates that the SPI is idle or disabled.
TFNF	1	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty location, and is clear when the FIFO is full.
TFE	2	Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. Otherwise, is clear. This bit does not request an interrupt.
RFNE	3	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries, and is clear when the receive FIFO is empty. This bit can be polled to completely empty the FIFO.
RFF	4	Receive FIFO Full. When the receive FIFO is completely full, this bit is set. Otherwise, it is clear.
TXE	5	Transmission Error. Set if the transmit FIFO is empty when a transfer is started.
DCOL	6	Data Collision Error. This bit is set if the ss_in_n input is asserted by another master, while in the middle of a transfer. The data would be halted before completion.

7.1.10 IMR

Setting	Position	Description
TXEIM	0	Receive FIFO Empty Interrupt Mask. 0: TXE_INTR interrupt is masked, 1: interrupt is not masked.
TXOIM	1	Transmit FIFO Overflow Interrupt Mask. 0: TXO_INTR interrupt is masked, 1: interrupt is not masked.
RXUIM	2	Receive FIFO Underflow Interrupt Mask. 0: RXU_INTR interrupt is masked, 1: interrupt is not masked.
RXIOM	3	Receive FIFO Overflow Interrupt Mask. 0: RXO_INTR interrupt is masked, 1: interrupt is not masked.
RXFIM	4	Receive FIFO Full Interrupt Mask. 0: RXF_INTR interrupt is masked, 1: interrupt is not masked.
MSTIM	5	Multi-Master Contention Interrupt Mask. 0: MST_INTR interrupt masked, 1: interrupt is not masked.

7.1.11 ISR

Setting	Position	Description
TXEIS	0	Receive FIFO Empty Interrupt Status. 0: TXE_INTR interrupt is not active after masking, 1: interrupt is active after masking.
TXOIS	1	Transmit FIFO Overflow Interrupt Status. 0: TXO_INTR interrupt is not active after masking, 1: interrupt is active after masking.
RXUIS	2	Receive FIFO Underflow Interrupt Status. 0: RXU_INTR interrupt is not active after masking, 1: interrupt is active after masking.
RXIOS	3	Receive FIFO Overflow Interrupt Status. 0: RXO_INTR interrupt is not active after masking, 1: interrupt is active after masking.
RXFIS	4	Receive FIFO Full Interrupt Status. 0: RXF_INTR interrupt is not active after masking, 1: interrupt is active after masking.
MSTIS	5	Multi-Master Contention Interrupt Status. 0: MST_INTR interrupt not active after masking, 1: interrupt is active after masking.

7.1.12 RISR

Setting	Position	Description
TXEIR	0	Receive FIFO Empty Raw Interrupt Status. 0: TXE_INTR interrupt is not active prior to masking, 1: interrupt is active prior to masking.
TXOIR	1	Transmit FIFO Overflow Raw Interrupt Status. 0: TXO_INTR interrupt is not prior to after masking, 1: interrupt is active prior to masking.
RXUIR	2	Receive FIFO Underflow Raw Interrupt Status. 0: RXU_INTR interrupt is not active prior to masking, 1: interrupt is active prior to masking.
RXIOR	3	Receive FIFO Overflow Raw Interrupt Status. 0: RXO_INTR interrupt is not active prior to asking, 1: interrupt is active prior to masking.
RXFIR	4	Receive FIFO Full Raw Interrupt Status. 0: RXF_INTR interrupt is not prior to after asking, 1: interrupt is active prior to masking.
MSTIR	5	Multi-Master Contention Raw Interrupt Status. 0: MST_INTR interrupt not active prior to masking, 1: interrupt is active prior to masking.

7.1.13 TXOICR

Setting	Position	Description
TXOICR	0	Clear Transmit FIFO Overflow Interrupt. Reflects the status of the interrupt. A read from this register clears the TXO_INTR interrupt. Writing has no effect.

7.1.14 RXOICR

Setting	Position	Description
RXOICR	0	Clear Receive FIFO Overflow Interrupt. Reflects the status of the interrupt. A read from this register clears the RXO_INTR interrupt. Writing has no effect.

7.1.15 RXUICR

Setting	Position	Description
RXUICR	0	Clear Receive FIFO Underflow Interrupt. Reflects the status of the interrupt. A read from this register clears the RXU_INTR interrupt. Writing has no effect.

7.1.16 MSTICR

Setting	Position	Description
MSTICR	0	Clear Multi-Master Contention Interrupt. Reflects The status of the interrupt. A read from this Register clears the MST_INTR interrupt. Writing has no effect.

7.1.17 ICR

Setting	Position	Description
ICR	0	Clear Interrupts. This register is set if any of these interrupts are active: TXO_INTR, RXU_INTR, RXO_INTR, or MST_INTR. A read from this register clears these interrupts. Writing has no effect.

7.1.18 DR

Setting	Position	Description
DR	0-31	Data Read/Write. Size is 16 or 32 bits depending transfer size. The corresponding read or write FIFO is accessed when this register is read or written to.

8. Inter-integrated Sound, I²S

Two I2S ports supporting Master mode are available. One of these ports is routed to the internal integrated CODEC, and is not connectable to external pins. The other I2S port is for external peripheral access. Below are the features:

- I2S transmitter and/or receiver based on the Philips I²S serial protocol.
- Configurable number of stereo channels (up to 4) for both transmitter and receiver.
- Full duplex communication due to the independence of transmitter and receiver.
- Asynchronous clocking of APB bus and I2S sclk.
- Master mode of operation.
- Audio data resolutions of 12, 16, 20, 24, and 32 bits per sample.
- FIFO depth of 16 samples.
- Programmable FIFO thresholds.

8.1. I²S Register Definitions

Register	Offset	Size	Description
IER	0x00	1b	I2S Enable
IRER	0x04	1b	Receiver Block Enable
ITER	0x08	1b	Receiver Block Enable
CER	0x0C	1b	Clock Enable
CCR	0x10	5b	Clock Configuration
RXFFR	0x14	1b	Receive FIFO Reset
TXFFR	0x18	1b	Transmit FIFO Reset
CHANNEL_0	0x20		Channel 0
CHANNEL_1	0x60		Channel 1
CHANNEL_2	0XA0		Channel 2
CHANNEL_3	0xE0		Channel 3
COMP_2	0x1F0	32b	Component Parameter 2 Register
COMP_1	0x1F4	32b	Component Parameter 1 Register

8.1.1 IER

Setting	Position	Description
IEN	0	A disable on this bit will override any other block or channel enables and will flush the FIFOs. 1: enable, 0: disable.

8.1.2 IRER

Setting	Position	Description
RXEN	0	Receiver block enable. 1: enable, 0: disable.

8.1.3 ITER

Setting	Position	Description
TXEN	0	Transmitter block enable. 1: enable, 0: disable.

8.1.4 CER

Setting	Position	Description

CLKEN	0	Clock generation enable/disable. 1: clock generation enable, 0: clock generation disable

8.1.5 CCR

Setting	Position	Description
SCLKG	0-2	Clock gating setting: 0: No clock gating 1: Gate after 12 clock cycles 2: Gate after 16 clock cycles 3: Gate after 20 clock cycles 4: Gate after 24 clock cycles This value should be greater than or equal to the largest configured audio resolution to prevent truncating RX/TX audio data.
WSS stays	3-4	Cycles for which word select line, ws_out, In the left or right sample mode: 0: 16 clock cycles 1: 24 clock cycles 2: 32 clock cycles The clock generation block must be disabled prior to any changes in this value.

8.1.6 RXFFR

Setting	Position	Description
RXFFR	0	Receive FIFO Reset. Writing a 1 to this register flushes all the RX FIFOs. This bit will self-clear.

8.1.7 TXFFR

Setting	Position	Description
TXFFR	0	Transmitter FIFO Reset. Writing a 1 to this register flushes all the TX FIFOs. This bit will self-clear.

8.1.8 COMP_2

Setting	Position	Description
RX_WSIZE_0	0-2	0: 12 bit resolution
RX_WSIZE_1	3-5	1: 16 bit resolution
Reserved	6	2: 20 bit resolution
RX_WSIZE_2	7-9	3: 24 bit resolution
RX_WSIZE_3	10-12	4: 32 bit resolution 5-7: reserved

8.1.9 COMP_1

Setting	Position	Description
APB_WIDTH 0-1		0: 8 bits, 1: 16 bits, 2: 32 bits
FIFO_DEPTH	2-3	0: 2 words, 1: 4 words, 2: 8 words, 3: 16 words
MODE_EN	4	0: disable, 1: enable
TX_BLOCK	5	0: disable, 1: enable

RX_BLOCK	6	0: disable, 1: enable
RX_CHANNELS	7-8	0-3: 1-4 channels
TX_CHANNELS	9-10	0-3: 1-4 channels
Reserved	11-15	
TX_WSIZE_0	16-18	0: 12 bit resolution
TX_WSIZE_1	19-21	1: 16 bit resolution
TX_WSIZE_2	22-24	2: 20 bit resolution
TX_WSIZE_3	25-27	3: 24 bit resolution
		4: 32 bit resolution

8.1.10 CHANNEL_X

8.1.10.1. LRBRx offset 0x00 size 32b Left Receive Buffer

Setting	Position	Description
RX_WORD	0-31	Right justified RX data for left channel

8.1.10.2. LTHRx offset 0x00 size 32b Left Transmit Holding

Setting	Position	Description
TX_WORD	0-31	Right justified TX data for left channel

8.1.10.3. RRBRx offset 0x04 size 32b Left Receive Buffer

Setting	Position	Description
RX_WORD	0-31	Right justified RX data for right channel

8.1.10.4. RTHRx offset 0x04 size 32b Left Transmit Holding

Setting	Position	Description
TX_WORD	0-31	Right justified TX data for right channel

8.1.10.5. RERx offset 0x08 size 1b Receive Enable

Setting	Position	Description
RXCHEN	0	Receive channel enable. Begins receiving on the next stereo cycle. 0: disable, 1: enable

8.1.10.6. TERx offset 0x0C size 1b Transmit Enable

Setting	Position	Description
TXCHEN	0	Transmit channel enable. Begins transmitting on the next stereo cycle. 0: disable, 1: enable

8.1.10.7. RCRx offset 0x10 size 3b Receive Configuration

Setting	Position	Description
WLEN	0-2	Resolution of the receiver. Channel must be disabled to change this setting. 0x0: ignore word length 0x1: 12 bit resolution 0x2: 16 bit resolution 0x3: 20 bit resolution 0x4: 24 bit resolution 0x5: 32 bit resolution

8.1.10.8. TCRx offset 0x14 size 3b Transmit Configuration

Setting	Position	Description
WLEN	0-2	Resolution of the transmitter. Channel must be

		disabled to change this setting. 0x0: ignore word length 0x1: 12 bit resolution 0x2: 16 bit resolution 0x3: 20 bit resolution 0x4: 24 bit resolution 0x5: 32 bit resolution

8.1.10.9. ISRx offset 0x18 size 6b Interrupt Status

Setting	Position	Description
RXDA	0	Status or Receive Data Available Interrupt. RX FIFO data available. 0: trigger level not reached, 1: trigger level reached.
RXFO	1	Status or RX channel Data Overrun. Incoming data lost due to full FIFO. 0: RX FIFO valid, 1: RX FIFO overrun.
Reserved	2-3	
TXFE	4	Status of Transmit Empty Trigger Interrupt. TX FIFO is empty. 0: trigger level not reached, 1: Trigger level reached.
TXFO	5	Status of TX channel Data Overrun. Attempt to write To full TX FIFO. 0: TX FIFO write valid, 1: TX FIFO write overrun.

8.1.10.10. IMRx offset 0x1C size 6b Interrupt Mask

Setting	Position	Description
RXDAM	0	Mask RX FIFO Data Available Interrupt. 0: unmask interrupt 1: mask interrupt
RXFOM	1	Mask RX FIFO Overrun Interrupt. 0: unmask interrupt 1: mask interrupt
Reserved	2-3	
TXFEM	4	Mask TX FIFO Data Empty Interrupt. 0: unmask interrupt 1: mask interrupt
TXFOM	5	Mask TX FIFO Overrun Interrupt. 0: unmask interrupt 1: mask interrupt

8.1.10.11. RORx offset 0x20 size 1b Receive Overrun

Setting	Position	Description
RXCHO	0	Read this bit to clear RX FIFO Data Overrun. 0: RX FIFO valid 1: RX FIFO overrun

8.1.10.12. TORx offset 0x24 size 1b Transmit Overrun

Setting	Position	Description
TXCHO	0	Read this bit to clear TX FIFO Data Overrun. 0: TX FIFO valid 1: TX FIFO overrun

8.1.10.13. RFCRx offset 0x28 size 4b Receive FIFO Configure

Setting	Position	Description
RXCHDT	0-3	Set the trigger level of the RX FIFO at which the Received Data Available interrupt is triggered. Trigger Level = RXCHDT value + 1, from 1-16.

8.1.10.14. TFCRx offset 0x2C size 4b Transmit FIFO Configure

Setting	Position	Description
TXCHET	0-3	Set the trigger level of the TX FIFO at which the Empty Threshold Reached interrupt is triggered. Trigger Level = TXCHDT value, from 0-15.

8.1.10.15. RFFx offset 0x30 size 1b Receive FIFO Flush

Setting	Position	Description
RXCHFR	0	RX channel FIFO reset. Write a 1 to this bit to flush the RX FIFO. This will self-clear. RX channel must be disabled prior to writing.

8.1.10.16. TFFx offset 0x34 size 1b TransmiT FIFO Flush

Setting	Position	Description
RXCHFR	0	TX channel FIFO reset. Write a 1 to this bit to flush the TX FIFO. This will self-clear. TX channel must be disabled or blocked prior to writing.

9. Two-wire Interface, I²C

One I2C port is available, supporting two-wire interface. Below are the features:

- Serial data line, SDA, and serial clock, CLK.
- Two speeds:
  - Standard <100 Kb/s
  - Fast 400 Kb/s
- Clock synchronization
- Master or slave I²C operation
- 7 or 10 bit addressing
- 7 or 10 bit combined format transfers
- Bulk transmit mode
- TX and RX buffers
- Interrupt or polled operation
- Handles bit and byte waiting

9.1. I²C Register Definitions

Register	Offset	Size	Description
CON	0x00	10b	I²C Control
TAR	0x04	13b	I²C Target Address
SAR	0x08	10b	I²C Slave Address
DATA_CMD	0x10	12b	RX/TX Buffer and Command
SS_SCL_HCNT	0x14	16b	Standard Speed Clock High Count
SS_SCL_LCNT	0x18	16b	Standard Speed Clock Low Count
FS_SCL_HCNT	0x1C	16b	Fast Mode Clock High Count
FS_SCL_LCNT	0x20	16b	Fast Mode Clock Low Count
INTR_STAT	0x2C	14b	Interrupt Status
INTR_MASK	0x30	14b	Interrupt Mask
RAW_INTR_STAT	0x34	14b	Raw Interrupt Status
RX_TL	0x38	3b	Receive FIFO Threshold
TX_TL	0x3C	3b	Transmit FIFO Threshold
CLR_INTR	0x40	1b	Clear Combined and Individual Interrupt
CLR_RX_UNDER	0x44	1b	Clear RX_UNDER Interrupt
CLR_RX_OVER	0x48	1b	Clear RX_OVER Interrupt
CLR_TX_OVER	0x4C	1b	Clear TX_OVER Interrupt
CLR_RD_REQ	0x50	1b	Clear RD_REQ Interrupt
CLR_TX_ABRT	0x54	1b	Clear TX_ABRT Interrupt
CLR_RX_DONE	0x58	1b	Clear RX_DONE Interrupt
CLR_ACTIVITY	0x5C	1b	Clear ACTIVITY Interrupt
CLR_STOP_DET	0x60	1b	Clear STOP_DET Interrupt
CLR_START_DET	0x64	1b	Clear START_DET Interrupt
CLR_GEN_CALL	0x68	1b	Clear GEN_CALL Interrupt
ENABLE	0x6C	3b	I²C Enable
STATUS	0x70	11b	Status
TXFLR	0x74	3b	Transmit FIFO Level
RXFLR	0x78	3b	Receive FIFO Level
SDA_HOLD	0x7C	24b	SDA Hold Time Length
TX_ABRT_SOURCE	0x80	32b	Transmit Abort Status
SLV_DATA_NACK_ONLY	0x84	1b	Generate SLV_DATA_NACK
SDA_SETUP	0x94	8b	SDA Setup
ACK_GENERAL_CALL	0x98	1b	ACK General Call
ENABLE_STATUS	0x9C	3b	Enable Status

CLR_RESTART_DET	0xA8	1b	Clear RESTART_DET Interrupt

9.1.1 CON

Setting	Position	Description
MASTER_MODE	0	This bit controls whether the I2C master is enabled. 1: enable, 0: disable.
SPEED	1-2	Speed of I2C operation, when master. 1: standard mode, 2: fast mode, 3: reserved
SADDR_SIZE	3	As a slave, sets either 7 or 10 bit address size. 0: 7 bit, 1: 10 bit
MADDR_SIZE	4	As a master, sets either 7 or 10 bit address size. 0: 7 bit, 1: 10 bit
RESTART_EN	5	As a master, determines if RESTART conditions are sent: sending a START BYTE, direction changes, read operation with 10 bit address. 0: disable, 1: enable
SLAVE_DIS	6	Disables the slave operation, must be set to 1 after reset to disable. 0: enable (default) 1: disable
STP_DET_ADDR	7	In slave mode, 0: issues STOP_DET irrespective of whether it's addressed or not 1: issues STOP_DET interrupt only when it is addressed.
EMPTY_CTRL	8	TX_EMPTY interrupt generated when set to 1.
FULL_HLD_CNT	9	Holds the bus when the RX FIFO is full to the buffer Depth when set to 1.
STP_DET_MAST	10	In master mode, 0: issues STOP_DET irrespective of whether the master is active, 1: issues the STOP_DET interrupt only when the master is active.

9.1.2 TAR

Setting	Position	Description
TAR	0-9	Target address for any master transaction. Ignored during a General Call.
GC_OR_START	10	If bit 11, SPECIAL, is set to 1, then this bit indicates whether a General Call or START byte is performed. 0: General Call Address – after issuing a General Call, only writes may be performed. I2C remains in General Call mode until SPECIAL bit is cleared, 1: START BYTE.
SPECIAL	11	Performs General Call or START BYTE command. 0: ignore bit 10 and use TAR normally, 1: perform special I2C command as specified in bit 10.
10BIT_MAST	12	As a master, starts transfers in 7 or 10 bit mode, 0: 7 bit, 1: 10 bit

9.1.3 SAR

Setting	Position	Description
SAR	0-9	Target address for slave.

9.1.4 DATA_CMD

Setting	Position	Description
DAT	0-7	Contains the data to be transmitted or receive on the I2C bus.
CMD	8	Determines if read or write is performed when in master mode. 0: Write, 1: Read.
STOP	9	Controls whether a STOP is issued after the byte is sent or received. Only available when EMPTYFIFO_HLD_MAST_EN is configured to 1. 0: STOP is not issued after this byte, regardless of whether or not the TX FIFO is empty, 1: STOP is issued after this byte, regardless of whether or not the TX FIFO is empty.
RESTART	10	Controls whether a RESTART is issued before the byte is sent/received. Only available when EMPTYFIFO_HLD_MAST_EN is configured to 1. 0: if RESTART_EN is a 1, RESTART is issued only if the transfer direction is changing from the previous Command, 1: a RESTART is issued before the data is Sent/received regardless of whether or not the transfer direction is changing.
FIRST_BYTE	11	Indicates the first data byte received after the Address phase for receive transfer in Master or Slave receiver mode. Available when FIRST_DATA_BYTE_STATUS is set to 1.

9.1.5 SS_SCL_HCNT

Setting	Position	Description
SS_SCL_HCNT	0-15	Must be set before transactions can take place. Sets the SCL clock high-period count for standard speed. Can be written only when ENABLE is set to 0. Minimum value is 6.

9.1.6 SS_SCL_LCNT

Setting	Position	Description
SS_SCL_HCNT	0-15	Must be set before transactions can take place. Sets the SCL clock low-period count for standard speed. Can be written only when ENABLE is set to 0. Minimum value is 8.

9.1.7 FS_SCL_HCNT

Setting	Position	Description

SS_SCL_HCNT	0-15	Must be set before transactions can take place. Sets the SCL clock high-period count for fast mode. Can be written only when ENABLE is set to 0. Minimum value is 6.

9.1.8 FS_SCL_LCNT

Setting	Position	Description
SS_SCL_HCNT	0-15	Must be set before transactions can take place. Sets the SCL clock low-period count for fast mode. Can be written only when ENABLE is set to 0. Minimum value is 8.

9.1.9 INTR_STAT

Setting	Position	Description
RX_UNDER	0	Indicates the status of these interrupts.
RX_OVER	1	
RX_FULL	2	
TX_OVER	3	
TX_EMPTY	4	
RD_REQ	5	
TX_ABRT	6	
RX_DONE	7	
ACTIVITY	8	
STOP_DET	9	
START_DET	10	
GEN_CALL	11	
RESTART_DET	12	
MST_ON_HOLD	13	

9.1.10 INTR_MASK

Setting	Position	Description
RX_UNDER	0	These bits mask the corresponding interrupt status
RX_OVER	1	bits in the INTR_STAT register.
RX_FULL	2	
TX_OVER	3	
TX_EMPTY	4	
RD_REQ	5	
TX_ABRT	6	
RX_DONE	7	
ACTIVITY	8	
STOP_DET	9	
START_DET	10	
GEN_CALL	11	
RESTART_DET	12	
MST_ON_HOLD	13	

9.1.11 RAW_INTR_STAT

Setting	Position	Description
RX_UNDER	0	
RX_OVER	1	

RX_FULL	2
TX_OVER	3
TX_EMPTY	4
RD_REQ	5
TX_ABRT	6
RX_DONE	7
ACTIVITY	8
STOP_DET	9
START_DET	10
GEN_CALL	11
RESTART_DET	12
MST_ON_HOLD	13

9.1.12 RX_TL

Setting	Position	Description
RX_TL	0-2	Sets the level of entries or above, that triggers the RX_FULL interrupt. Threshold = entry value + 1.

9.1.13 TX_TL

Setting	Position	Description
TX_TL	0-2	Sets the level of entries or below, that triggers the TX_EMPTY interrupt. Range is 0-7.

9.1.14 CLR_INTR

Setting	Position	Description
CLR_INTR	0	Read this register to clear the combined, all Individual, and TX_ABRT_SOURCE interrupts.

9.1.15 CLR_RX_UNDER

Setting	Position	Description
CLR_RX_UNDER	0	Read this register to clear RX_UNDER.

9.1.16 CLR_RX_OVER

Setting	Position	Description
CLR_RX_OVER	0	Read this register to clear RX_OVER.

9.1.17 CLR_RD_REQ

Setting	Position	Description
CLR_RD_REQ	0	Read this register to clear RD_REQ.

9.1.18 CLR_TX_ABRT

Setting	Position	Description
CLR_TX_ABRT	0	Read this register to clear TX_ABRT.

9.1.19 CLR_RX_DONE

Setting	Position	Description
CLR_RX_DONE	0	Read this register to clear RX_DONE.

9.1.20 CLR_ACTIVITY

Setting	Position	Description
CLR_ACTIVITY	0	Read this register to clear ACTIVITY interrupt.

9.1.21 CLR_STOP_DET

Setting	Position	Description
CLR_ACTIVITY	0	Read this register to clear STOP_DET interrupt.

9.1.22 CLR_START_DET

Setting	Position	Description
CLR_ACTIVITY	0	Read this register to clear START_DET interrupt.

9.1.23 CLR_GEN_CALL

Setting	Position	Description
CLR_ACTIVITY	0	Read this register to clear GEN_CALL interrupt.

9.1.24 IC_ENABLE

Setting	Position	Description
ENABLE	0	Enables the I2C interface when set to 1. Before disabling, must flush the TX/RX FIFO.
ABORT	1	When set to 1, aborts the transfer: issues a STOP and flushes the TX FIFO after the current transfer is complete. This bit is cleared automatically.
TX_CMD_BLOCK	2	In Master mode, blocks the transmission of data when set to 1. When set to 0, starts transmission of data when available in the TX FIFO.

9.1.25 IC_STATUS

Setting	Position	Description
ACTIVITY	0	I^2C Activity Status
TFNF	1	TX FIFO contains one or more empty locations when set to 1.
TFE	2	TX FIFO is completely empty when set to 1.
RFNE	3	RX FIFO contains one or more entries when set to 1.
RFF	4	RX FIFO is completely full when set to 1.
MST_ACTIVITY	5	When Master is not in IDLE, this bit is set to 1.
SLV_ACTIVITY	6	When Slave is not in IDLE, this bit is set to 1.

MST_HOLD_TXE	7	If EMPTY_HOLD_MASTER_EN is set to 1, this will stall The write transfer when TX FIFO is empty, and the last byte does not have the STOP bit set.
MST_HOLD_RXF	8	Indicates the BUS hold in Master mode due to RX FIFO is full and additional data has been received.
SLV_HOLD_TXE	9	Indicates the BUS hold in Slave mode for the read request when the TX FIFO is empty. The bus is in hold until the TX FIFO has data to transmit for the read request.
SLV_HOLD_RXF	10	Indicates the BUS hold in Slave mode due to RX FIFO being full and additional data received.

9.1.26 TXFLR

Setting	Position	Description
TXFLR	0-2	Contains the number of valid entries in the TX FIFO.

9.1.27 RXFLR

Setting	Position	Description
RXFLR	0-2	Contains the number of valid entries in the RX FIFO.

9.1.28 SDA_HOLD

Setting	Position	Description
SDA_TX_HOLD	0-15	Sets the required SDA hold time in clock periods as a transmitter.
SDA_RX_HOLD	15-23	Sets the required SDA hold time in clock periods as a receiver.

9.1.29 ABRT_SOURCE

Setting	Position	Description
ABRT7B_ADDR_NK	0	Master in 7-bit address mode, address was not acked by any slave.
ABRT10B_ADDR1_NK	1	Master in 10-bit address mode, first 10-bit address byte was not acked by any slave.
ABRT10B_ADDR2_NK	2	Master in 10-bit address mode, second 10-bit address byte was not acked by any slave.
ABRT_TXDATA_NK	3	Master transmission did not receive an ack from slave.
ABRT_GCALL_NK	4	Master mode sends a General Call and no slave acked.
Reserved	5-6	
ABRT_START_ACK	7	Master sends a START byte and the slave incorrectly acked this byte.
Reserved	8-22	

TX_FLUSH_CNT	23-21	Number of TX FIFO data commands that are flushed due to TX_ABRT interrupt. Cleared with I²C is disabled.

9.1.30 SLV_DATA_NACK_ONLY

Setting	Position	Description
NACK	0	Generate NACK as a slave when set to 1. When set to 0, a NACK or ACK is generated normally.

9.1.31 SDA_SETUP

Setting	Position	Description
SDA_SETUP	0-7	SDA Setup. Number of clock periods introduced in the rising edge of the SCL, relative to SDA changing, by holding SCL low when the I²C services a read request while a slave-transmitter. Minimum is 2; default is 0x64.

9.1.32 ACK_GENERAL_CALL

Setting	Position	Description
ACK_GEN_CALL	0	Ack General Call. When set to 1, the I²C responds with an ACK when it receives a General Call. When set to 0, the I²C does not generate General Call interrupts.

9.1.33 ENABLE_STATUS

Setting	Position	Description
EN	0	I2C Enable Status. When a 1, I²C is in enabled state. When a 0, I²C is inactive.
SLV_DIS_BUSY	1	Slave Disabled While Busy. This bit indicates if a potential or active slave operation has been aborted due to setting bit 0 in the ENABLE register from 1 to 0.
SLV_RX_LOST	2	Slave Received Data Lost. Indicates when a slave-receiver operation has been aborted with at least one data byte received.

9.1.34 CLR_RESTART_DET

Setting	Position	Description
CLR_RESTART_DET	0	Read this bit to clear the RESTART_DET interrupt.

10. UART Interface

Up to 3 UART ports (UART0, 1 and 2) are available in the ACH. Control registers are mapped to the APB bus. The following features are supported:

- Transmit and Receive FIFO of 256 Bytes
- Support industry-standard 16550
- Auto Flow Control with RTS/CTS hardware pin
- Programmable interrupts for Tx and Rx FIFO
- Programmable fractional baud rate support

10.1. UART Register Definition

Register	Offset	Size	Description
RBR	0x00	9b	Receive Buffer Register
THR	0x00	9b	Transmit Holding Register
DLL	0x00	8b	Divisor Latch (Low)
DLH	0x04	8b	Divisor Latch (High)
IER	0x04	8b	Interrupt Enable Register
IIR	0x08	8b	Interrupt Identification Register
FCR	0x08	8b	FIFO Control Register
LCR	0x0C	8b	Line Control Register
MCR	0x10	6b	Modem Control Register
LSR	0x14	9b	Line Status Register
MSR	0x18	8b	Modem Status Register
FAR	0x70	1b	FIFO Access Register
TFR	0x74	8b	Transmit FIFO Read
RFW	0x78	10b	Receive FIFO Write
USR	0x7C	5b	UART Status Register
TFL	0x80	9b	Transmit FIFO Level
RFL	0x84	9b	Receive FIFO Level
SRR	0x88	3b	Software Reset Register
DLF	0xC0	4b	Divisor Latch Fractional Value.

10.1.1 RBR

Setting	Position	Description
RX	0-7	Receive Buffer Register (LSB 8 bit)
RX	8	Receive Buffer Register (MSB 9th Bit)

10.1.2 THR

Setting	Position	Description
TX Register	0-7	Transmit Hold Register (LSB 8 bit)
TX Register	8	Transmit Hold Register (MSB 9th Bit)

10.1.3 DLL

Setting	Position	Description
DIV_LATCH	0-7	Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART.

10.1.4 DLH

Setting	Position	Description
DIV_LATCH	0-7	Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART.

10.1.5 IER

Setting	Position	Description
ERBFI	0	Enable Received Data Available Interrupt. 0: disable 1: enable
ETBEI	1	Enable Transmit Holding Register Empty Interrupt 0: disable 1: enable
ELSI	2	Enable Receiver Line Status Interrupt 0: disable 1: enable
EDSSI	3	Enable Modem Status Interrupt 0: disable 1: enable
Reserved	4-6	
PTIME	7	Programmable THRE Interrupt Mode Enable 0: disable 1: enable

10.1.6 IIR

Setting	Position	Description
INTR_ID	0-3	Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout
Reserved	4-5	
FIFOSE	6-7	FIFOs Enabled 0: disable 1: enable

10.1.7 FCR

Setting	Position	Description
FIFOE	0	FIFO Enable
RFIFOR	1	Receive FIFO Reset
XFIFOR	2	XMIT FIFO Reset
Reserved	3	
TET	4-5	TX Empty Trigger
RT	6-7	RCVR Trigger

10.1.8 LCR

Setting	Position	Description
DLS	0-1	Data Length Select. The number of bits that may be selected are as follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
STOP	2	Number of Stop Bits 0: 1 stop bit 1: 1.5 stop bits when DLS is 0, else 2 stop bit
PEN	3	Parity Enable 0: disabled 1: enabled
EPS	4	Even parity select
STICK_PARITY	5	Stick Parity 0: disabled 1: enabled
BC	6	Break Control Bit. Causes a break on the receiving device when set to 1
DLAB	7	Divisor Latch Access Bit

10.1.9 MCR

Setting	Position	Description
DTR	0	Data Terminal Ready
RTS	1	Request to Send
Reserved	2-3	
LB	4	Loop Back Bit
AFCE	5	Auto Flow Control Enable 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled

10.1.10 LSR

Setting	Position	Description
DR	0	Data Ready Bit 0: no data ready 1: data ready
OE	1	Overrun error bit 0: no overrun error 1: overrun error
PE	2	Parity error bit 0: no parity error 1: parity error
FE	3	Framing error bit 0: no framing error 1: framing error
BI	4	Break interrupt bit
THRE	5	Transmit Holding Register Empty bit
TEMT	6	Transmitter Empty bit.

RFE	7	Receive FIFO error bit 0: no error in RX FIFO 1: error in RX FIFO
ADDR_RCVD	8	Address Received bit 0: Indicates that the character is data. 1: Indicates that the character is an address.

10.1.11 MSR

Setting	Position	Description
DTCS	0	Delta Clear to Send 0: no change on CTS since last read of MSR 1: change on CTS since last read of MSR
DDSR	1	Delta Data Set Ready. 0: no change on DSR since last read of MSR 1: change on DSR since last read of MSR
TERI	2	Trailing Edge of Ring Indicator. 0: no change on RI since last read of MSR 1: change on RI since last read of MSR
DDCD	3	Delta Data Carrier Det 0: no change on DCD since last read of MSR 1: change on DCD since last read of MSR
CTS	4	Clear to Send 0: CTS input is de-asserted (logic 1) 1: CTS input is asserted (logic 0)
DSR	5	Data Set Ready 0: DSR input is de-asserted (logic 1) 1: DSR input is asserted (logic 0)
RI	6	Ring Indicator 0: RI input is de-asserted (logic 1) 1: RI input is asserted (logic 0)
DCD	7	Data Carrier Detect 0: DCD input is de-asserted (logic 1) 1: DCD input is asserted (logic 0)

10.1.12 FAR

Setting	Position	Description
FIFO_ACCESS	0	FIFO access mode. 0: FIFO access mode disabled 1: FIFO access mode enabled

10.1.13 TFR

Setting	Position	Description
TX_FIFO_RD	0-7	Read the data at the top of the transmit FIFO. Each read pops the TX FIFO and gives the next data value which was moved to the top of the FIFO.

10.1.14 RFW

Setting	Position	Description
RFWD	0-7	Data written to the RFWD is pushed to the RX FIFO. Each write pushes new data to the next write location in the RX FIFO.
RFPE	8	RX FIFO Parity Error.
RFFE	9	RX FIFO Framing Error.

10.1.15 USR

Setting	Position	Description
BUSY	0	UART Busy 0: UART is idle or inactive 1: UART is busy (transferring data)
TFNF	1	Transmit FIFO not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
TFE	2	Transmit FIFO Empty 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
RFNE	3	Receive FIFO Not Empty 0: Receive FIFO is empty 1: Receive FIFO is not empty
RFF	4	Receive FIFO full. 0: Receive FIFO not full 1: Receive FIFO full

10.1.16 TFL

Setting	Position	Description
TXFIFO	0-8	TX FIFO Level

10.1.17 RFL

Setting	Position	Description
RXFIFO	0-8	RX FIFO Level

10.1.18 SRR

Setting	Position	Description
UR	0	UART reset
RFR	1	RCVR FIFO Reset
XFR	2	XMIT FIFO Reset

10.1.19 DLF

Setting	Position	Description
DLF	0-3	Fractional part of divisor

Value	Fraction	Fractional Value
0000	0/16	0.0000
0001	1/16	0.0625
0010	2/16	0.125

0011	3/16	0.1875
0100	4/16	0.25
0101	5/16	0.3125
0110	6/16	0.375
0111	7/16	0.4375
1000	8/16	0.5
1001	9/16	0.5625
1010	10/16	0.625
1011	11/16	0.6875
1100	12/16	0.75
1101	13/16	0.8125
1110	14/16	0.875
1111	15/16	0.9375

11. GPIO

Up to 12 GPIO (GPIO0 ~ GPIO11) are available in the ACH. The following features are supported:

- Three ports, A to C, which are separately configurable.
- Separate data registers and data direction registers for each signal.
- Independently controllable signal bits.
- Configurable interrupt mode for Port A.
- Option to generate single or multiple interrupts.

11.1. GPIO Port Mapping

The following table details the mapping of each GPIO ID number to the corresponding GPIO Port location:

Table 2. GPIO ID to Port mapping

GPIO ID	Port location
GPIO0	PortA bit0
GPIO1	PortA bit1
GPIO2	PortA bit2
GPIO3	PortA bit3
GPIO4	PortB bit0
GPIO5	PortB bit1
GPIO6	PortB bit2
GPIO7	PortB bit3
GPIO8	PortC bit0
GPIO9	PortC bit1
GPIO10	PortC bit2
GPIO11	PortC bit3

11.2. GPIO Register Definitions

Register	Offset	Size	Description
SWPORTA_DR	0x00	4b	Port A data
SWPORTA_DDR	0x04	4b	Port A data direction
SWPORTA_CTL	0x08	4b	Port A data source
SWPORTB_DR	0x0c	4b	Port B data
SWPORTB_DDR	0x10	4b	Port B data direction
SWPORTB_CTL	0x14	4b	Port B data source
SWPORTC_DR	0x18	4b	Port C data
SWPORTC_DDR	0x1c	4b	Port C data direction
SWPORTC_CTL	0x20	4b	Port C data source
INT_EN	0x30	4b	Port A interrupt enable
INT_MASK	0x34	4b	Port A interrupt mask
INT_LEVEL	0x38	4b	Port A interrupt level
INT_POLARITY	0x3c	4b	Port A interrupt polarity
INT_STATUS	0x40	4b	Port A interrupt status
RAW_INT_STATUS	0x44	4b	Raw interrupt status of Port A
DEBOUNCE	0x48	4b	Debounce enable

PORTA_EOI	0x4c	4b	Port A clear interrupt
EXT_PORTA	0x50	4b	Port A external port
EXT_PORTB	0x54	4b	Port B external port
EXT_PORTC	0x58	4b	Port C external port
LS_SYNC	0x60	1b	Level-sensitive synchronization enable
INT_BOTHEDGE	0x68	4b	Interrupt both edge type

11.2.1 SWPORTA_DR

Setting	Position	Description
DATA	0-3	Values written to this register are output if the corresponding data direction bits for the Port are set to Output mode. The value read back is the last value written to this register.

11.2.2 SWPORTA_DDR

Setting	Position	Description
DATA_DIR	0-3	Values written to this register independently control the direction of the corresponding data bit in the Port. 0: Input 1: Ouput

11.2.3 SWPORTA_CTL

Setting	Position	Description
DATA_SOURCE	0-3	The data and control source for a GPIO comes from either software or hardware. This bit selects between them. In HW Mode, and if PORTA_SINGLE_CTL = 0, the Default value is replicated across all bits at startup. 0: SW Mode (default) 1: HW Mode

11.2.4 SWPORTB_DR

Setting	Position	Description
DATA	0-3	Values written to this register are output if the corresponding data direction bits for the Port are set to Output mode. The value read back is the last value written to this register.

11.2.5 SWPORTB_DDR

Setting	Position	Description
DATA_DIR	0-3	Values written to this register independently control the direction of the corresponding data bit in the Port. 0: Input

1: Ouput

11.2.6 SWPORTB_CTL

Setting	Position	Description
DATA_SOURCE	0-3	The data and control source for a GPIO comes from either software or hardware. This bit selects between them. In HW Mode, and if PORTC_SINGLE_CTL = 0, the Default value is replicated across all bits at startup. 0: SW Mode (default) 1: HW Mode

11.2.7 SWPORTC_DR

Setting	Position	Description
DATA	0-3	Values written to this register are output if the corresponding data direction bits for the Port are set to Output mode. The value read back is the last value written to this register.

11.2.8 SWPORTC_DDR

Setting	Position	Description
DATA_DIR	0-3	Values written to this register independently control the direction of the corresponding data bit in the Port. 0: Input 1: Ouput

11.2.9 SWPORTC_CTL

Setting	Position	Description
DATA_SOURCE	0-3	The data and control source for a GPIO comes from either software or hardware. This bit selects between them. In HW Mode, and if PORTC_SINGLE_CTL = 0, the Default value is replicated across all bits at startup. 0: SW Mode (default) 1: HW Mode

11.2.10 INT_EN

Setting	Position	Description
INT_ENABLE	0-3	Allows each bit of Port A to be configured for interrupts, disabled by default. A value 1 configures the corresponding bit in Port A to be an interrupt, and if the PORTA_DDR bit is set for input. data and control source for a GPIO comes from either software or hardware. This bit selects between them. In HW Mode, and if PORTC_SINGLE_CTL = 0, the Default value is replicated across all bits at startup. 0: Normal GPIO (default) 1: Interrupt Mode

11.2.11 INT_MASK

Setting	Position	Description
INT_ENABLE	0-3	Control whether an interrupt on Port A can create an interrupt by not masking it. By default, all interrupt bits are unmasked. A value of 1 in a bit, masks the corresponding interrupt. 0: Unmasked (default) 1: Masked

11.2.12 INT_LEVEL

Setting	Position	Description
INT_LEVEL	0-3	Controls the type of interrupt that occurs on a Port A bit. A value 0 configures the type to be level-sensitive, otherwise it is edge-sensitvie. 0: Level (default) 1: Edge

11.2.13 INT_POLARITY

Setting	Position	Description
INT_POLARITY	0-3	Controls the polarity of the edge or level for an interrupt on Port A. 0: Active-low (default) 1: Active-high

11.2.14 INT_STATUS

Setting	Position	Description
INT_STATUS	0-3	Interrupt status of Port A, post-mask.

11.2.15 RAW_INT_STATUS

Setting	Position	Description
RAW_STATUS	0-3	Interrupt status of Port A, pre-mask.

11.2.16 INT_DEBOUNCE

Setting	Position	Description
DEB_EN	0-3	Controls whether an external interrupt signal needs to be debounced to remove spurious glitches. A value 1 enables debouncing on the corresponding interrupt bit. A signal must be valid for two clock periods to be validated. 0: No debounce (default) 1: Enable

11.2.17 PORTA_EOI

Setting	Position	Description
INT_CLEAR	0-3	Clears an edge type interrupt on Port A. A value of 1 written clears the corresponding interrupt. 0: No interrupt clear 1: Clear

11.2.18 EXT_PORTA

Setting	Position	Description
EXT_PORTA	0-3	This register always reflects the signals on the external Port.

11.2.19 EXT_PORTB

Setting	Position	Description
EXT_PORTB	0-3	This register always reflects the signals on the external Port.

11.2.20 EXT_PORTC

Setting	Position	Description
EXT_PORTC	0-3	This register always reflects the signals on the external Port.

11.2.21 INT_BOTHEDGE

Setting	Position	Description
BOTHEDGE	0-3	Control an edge type interrupt on Port A. A value of 1 enables both falling and rising edges to generate interrupts for the corresponding bit. A value 0, default, allows the INT_TYPE and INT_POLARITY bits to control the interrupt instead.

12. Timer

4 Timers (TIM0 – TIM3) are available in the ACH. The following features are supported:

- 32 bit width
- 4 interrupt vectors
- Free-running or user defined mode

12.1. Address Ranges

Timer	Offset range
TIM0	0x00 to 0x10
TIM1	0x14 to 0x24
TIM2	0x28 to 0x38
TIM3	ox3c to 0x4c

12.2. Timer N Register Definitions

Register	Offset	Size	Description
LOAD_COUNT	0x00	32b	Value to be loaded into the TIM N. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.
CURRENT_VALUE	0x04	32b	Current Value of TIM N.
CONT_REG	0x08	3b	Value to be loaded into the TIM N. 0: ENABLE, Timer enable bit for TIM N. 0: disable 1: enable 1: COUNT_MODE 0: free-running mode, must set LOAD_CNT to 0xFFFFFFFF before enabling. 1: user-defined mode, uses LOAD_CNT register 2: INT_MASK 0: TIM N not masked 1: TIM N masked 31-3: Reserved
EOI	0x0C	1b	End of interrupt register. Reading from this register returns all zeroes and clears the interrupt from TIM N.
INT_STATUS	0x10	1b	Contains the interrupt status for TIM N.

13.Audio CODEC

An integrated audio CODEC is available in the ACH. Control registers are mapped to the APB bus. Audio data is sent using a dedicated I^2S port. The following features are supported:

- 24-bit D/A and A/D conversion.
- 90dB Dynamic Range and -80dB THD A/D Conversion.
- 96dB Dynamic Range and -86dB THD D/A Conversion.
- 2 Stereo Single-Ended/Differential Line-in and Microphones inputs.
- 1 Stereo Single-Ended Headset Driver.
- Built-in Microphone Bias.
- Built-in References and Biasing Circuitry.
- Analogue and Digital Gain with Soft-ramp Control.
- Input Automatic Volume Control (ALC).
- Power-on/off Pop-Suppression.
- Supported Audio Sampling Rates from 8 to 192 kHz.
- LPC standard I2S audio data interface in Master and Slave Mode Operation.

14. Clock specifications

The ACH1190 uses two clocks: a reference clock and an optional low power clock. For the reference clock, the ACH1190 can either use an external reference clock source or generate its own reference using a XTAL. The low-power clock must always be supplied from an external source.

Table 3. Main crystal specifications

Symbol	Parameter	Min	Typ	Max	Unit
External crystal					
F_{IN}	Clock input frequency list		26		MHz
F_{INTOL}	Tolerance on input frequency (typical)	-20	-	+20	ppm

Table 4. Low power clock specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequencies		32.768		kHz
F_{INTOL}	Tolerance on input frequency	-1000	-	+1000	ppm

15. Low power mode

The ACH1190 may run in low power mode using the optional 32KHz clock. The steps to enter and exit low power mode are the following:

- Setup: allow at least one interrupt to run in order to wake up the CPU core.
- Set ARM core to low power state.
- Select the 32KHz clock for the system clock and disable 26MHz main clock.
- Shut off PLL, ADC, and CODEC power.
- Keep SRAM enabled.
- Enter WFI mode to go to sleep.

Next, wake up from sleep:

- Set ARM to run mode.
- Enable 26MHz main clock.
- Select 26Mhz for the system and bus clock.
- Turn on: PLLs, ADC, and CODEC.
- Select PLL0 for ARM core and bus clock after it “locks”.

15.1. Register usage example

15.1.1 ARM core low power state

SCR register: set bits 4 and 2, clear bit 1

```
Bit 4 SEVONPEND Send Event on Pending bit:
   0 = only enabled interrupts or events can wakeup the processor, disabled
   interrupts are
   excluded
   1 = enabled events and all interrupts, including disabled interrupts, can
   wakeup the
   processor.
   When an event or interrupt enters pending state, the event signal wakes
   up the processor
   from WFE. If the processor is not waiting for an event, the event is
   registered and affects the
   next WFE.
   The processor also wakes up on execution of an SE V instruction or an
   external event.
Bit 2 SLEEPDEEP Controls whether the processor uses sleep or deep sleep as
its low power mode:
   0 = sleep
   1 = deep sleep.
Bit 1 SLEEPONEXIT Indicates sleep-on-exit when returning from Handler mode
to Thread mode:
   0 = do not sleep when returning to Thread mode.
   1 = enter sleep, or deep sleep, on return from an ISR.
   Setting this bit to 1 enables an interrupt driven application to avoid
   returning to an empty
   main application
```

15.1.2 Select 32KHz clock

SYSCFG register
CFG28, offset 0x74: set bit 0, clear bit 1:3

0x74	sys_cfg_reg28	default value
0	Select clock for the ARM processor 0, select the output of pll0 1, select input 32k clock, OSC32_IN To read this bit read register sys_cfg_reg39[28]	0
1	26MHz Oscillator IO is enable OSC_IN, OSC_OUT is 0, input clock is disable To read this bit read register sys_cfg_reg39[29]	1
2:3	26MHz Oscillator IO Drive Current To read this bit read register sys_cfg_reg39[31:30]	b11
31:4	Reserved	0

15.1.3 Turn off peripherals: PLLs, ADC, CODEC

SYSCFG register
CFG19, offset 0x50: clear bit 24

0x50	sys_cfg_reg19, pll0_reg1	default value
[23:0]	frac_0, Fractional part of feedback divide	0x13b13b;
24	pd_0, Global power down	0
25	dacpd_0, power down noise cancelling DAC	0
26	dsmpd_0, power down delta sigma modulator	0
27	foutpostdivpd_0, postdivide power down	0
28	fout4phasepd_0, powerdown 4 phase clock generator	0
29	foutvcopd_0, power down vco	0
30	bypass_0, bypass Pll, output will be refclock	0
31	Reserved	0

SYSCFG register
CFG22, offset 0x5C: clear bit 24

0x5C	sys_cfg_reg22, pll1_reg1	default value
[23:0]	frac_1, Fractional part of feedback divide	0x287cc5
24	pd_1, gloabal power down	1
25	dacpd_1, power down noise cancelling DAC	0
26	dsmpd_1, power down delta sigma modulator	0
27	foutpostdivpd_1, post divide power down	0
28	fout4phasepd_1, power down 4 phase clock generator	0
29	foutvcopd_1, power down vco	0
30	bypass_1, bypass PLL	0
31	Reserved	0

ADC0 and ADC1 registers (two registers)
offset 0xDC: set bit 0 in each register

0xDC	adc_wdt_configid_7	default value

0	PD	0

CODEC register (no register map provided)
Using API:

```
codec_reg_write_byte(18, 0);
codec_reg_write_byte(21, 0);
codec_reg_write_byte(22, 0);
codec_reg_write_byte(24, 0);
codec_reg_write_byte(26, 0);
```

15.1.4 Enable SRAM clock

SYSCFG register
CFG39, offset 0xA0: set bits 17:24

0xA0	sys_cfg_reg39, clock_enable	default value
0	dmac_ahb_pclk_en, Enables DMAC AHB interface clock	1
1	spi0_apb0_pclk_en, Enables SPI0 APB0 interface clock	1
2	spi1_apb0_pclk_en, Enables SPI1 APB0 interface clock	1
3	i2s0_apb0_pclk_en, I2S0 APB0 and serial interface clock	1
4	uart0_abp0_pclk_en, Enables UART0 APB0 interface clock	1
5	uart1_apb0_pclk_en, Enables UART1 APB0 interface clock	1
6	i2s1_apb0_pclk_en, I2S1 codec APB0 and serial interface clock	1
7	spi2_apb0_pclk_en, Enables SPI2 APB0 interface clock	1
8	i2c0_apb0_pclk_en, Enables I2C0 APB0 interface clock	1
9	wdt_apb1_pclk_en, Enables WDT APB1 interface clock	1
10	adc0_apb1_pclk_en, Enables ADC0 APB1 interface clock	1
11	adc1_apb1_pclk_en, Enables ADC1 APB1 interface clock	1
12	aes_apb1_pclk_en, Enables AES APB1 interface clock	1
13	uart2_apb0_pclk_en, Enables UART2 APB0 interface clock	1
14	in_osc26_pll0_en, Enables input 26MHz clock to Pll0 input clock	1
15	in_osc26_pll1_en, Enables input 26MHz clock to Pll1 input clock	1
16	codec_pclk_en, Enables CODEC APB0 interface clock	1
17	SRAM clk enable address for 0 to 64k	1
18	SRAM clk enable address for 64k to 192k	1
19	SRAM clk enable address for 192k to 320k	1
20	SRAM clk enable address for 320k to 448k	1
21	SRAM clk enable address for 448k to 576k	1
22	SRAM clk enable address for 576k to 704k	1
23	SRAM clk enable address for 704k to 832k	1
24	SRAM clk enable address for 832k to 960k	1
25	gpio0_pclk_en, Enables GPIO 0 interface clock	1
26	gpio1_pclk_en, Enables GPIO 1 interface clock	1
27	gpio2_pclk_en, Enables GPIO 2 interface clock	1
31:28	When reading this register, bit from sys_cfg_reg28[3:0] assigned	

15.1.5 Wakeup ARM core

SCR register: clear bit 2

15.1.6 Enable 26MHz clock

SYSCFG register
CFG28, offset 0x74: set bits 1:3

15.1.7 Select 26MHz system and bus clock

SYSCFG register
CFG2, offset 0xC: clear bit 4

0xC	sys_cfg_reg2, clock_control_reg0	default value
1:0	Reserved	0
3:2	Reserved	0
4	Select ARM and AHB Bus clock 0, selects input in_osc_clk_26MHz 1, selects PLL0 output clock MCO output 0, selects input in_osc_clk_26MHz 1, selects s1_pclk a APB1 clock	0
31:5	Reserved	0

15.1.8 Turn on PLLs

SYSCFG register
CFG19, offset 0x50: set bit 24

SYSCFG register
CFG22, offset 0x5C: set bit 24

15.1.9 Enable clocks

SYSCFG register
CFG39, offset 0xA0: set bits 0:27

15.1.10 Wait for PLL to lock ARM core

SYSCFG register
CFG32, offset 0x84: read bit 0, wait for set status

0x84	sys_cfg_reg32, clock_status	default value
0	boot, 0, Normal mode boot from ROM 1, Test mode, uart cmd to load bootloader	read from pin
1	Pll0_lock	read status
2	pll1_lock	read status
31:3	Reserved	reserved

15.1.11 Select PLL0 for ARM core clock

SYSCFG register
CFG28, offset 0x74: clear bit 0

15.1.12 Select PLL0 as system and bus clock

SYSCFG register
CFG2, offset 0xC: set bit 4

16.AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU and DMA) and slaves APB peripherals and ensures an efficient seamless operation even when several high-speed peripherals work simultaneously.

17. Embedded SRAM

Up to 960K bytes of system SRAM available for code and data RAM. RAM memory is accessed (read/write) at CPU clock speed. It can be enable/disable through clock gating to reduce the power consumption.

18.Electrical Characteristics

18.1. Absolute maximum ratings

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 5. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Digital Supply voltages	-0.3	+3.3	V
V_{CCA_PLL}	Analog PLL Supply voltage	-0.3	+3.6	V
V_{CC_HP}	Supply voltage I/O	-0.3	+3.6	V
$V_{CCA\_MAIN\_PLL}$	Supply voltage I/O	-0.3	+3.6	V
V_{in}	Input voltage on any digital pin	-0.3	+3.3	V
V_{ssdiff}	Maximum voltage difference between different types of Vss pins	-0.3	+0.3	V
T_{stg}	Storage temperature	-65	+100	°C

18.2. Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 6. Operating ranges

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating ambient temperature	-30	+25	+70	°C
V_{DD}	Digital Supply Voltage	+1.8	+2.5	+3.3	V
V_{CCA_PLL}	Analog Audio PLL Supply Voltage	+1.8	+2.5	+3.6	V
V_{CC_HP}	Analog Headset Supply Voltage	+2.5	+3.3	+3.6	V

$V_{CCA\_MAIN\_PLL}$	Analog Main PLL Supply Voltage	+1.8	+3.3	+3.6	V

18.3. Digital I/O specifications

All I/Os, except analog I/Os or otherwise specified are standard I/Os with levels complying with the EIA/JEDEC standard JESD8-7.

Table 7. DC and AC input specifications

Symbol	Parameter	Min	Typ	Max	Unit
Input levels					
V_{IL}	Low-level input voltage	0	-	0.35 * V_{DD_IO}	V
V_{IH}	High-level input voltage	0.65 * V_{DD_IO}	-	-	V
V_{hyst}	Schmitt trigger hysteresis	150	-	-	mV
T_r/T_f	Rise and fall time that can be present on inputs	-	-	25	ns
R_i	Input resistance	1	-	-	MΩ
C_i	Input capacitance	-	-	5	pF
Output levels					
V_{OL}	Low-level output voltage (@ +100 µA)	0	-	0.2	V
V_{OH}	High-level output voltage (@ -100 µA)	V_{DD_IO} - 0.2	-	V_{DD_IO}	V
T_r/T_f	Rise and fall time that can be present on outputs at Cload = 20 pF max	-	-	10	ns

Table 8. Pull-up and pull-down characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PU}	Equivalent pull-up resistance	V_{DD_IO} = 0 V	-	50	-	kΩ
R_{PD}	Equivalent pull-down resistance	V_{DD_IO} = 1.8 V	-	50	-	kΩ

Table 9. IOL and IOH characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	Sink current	V_{OL} = Max	X[1]	-	-	mA
I_{OH}	Source current	V_{OH} = Min	X[1]	-	-	mA

1. X can be 2, 4, or 8 depending on the type of the I/O (X denotes the drive strength of output stage).

Note: If the V_{DD_IO} supply is powered down, external activity on the IOs is not allowed.

18.4. Current consumption

All I/Os, except analog I/Os or otherwise specified are standard I/Os with levels complying with the EIA/JEDEC standard JESD8-7.

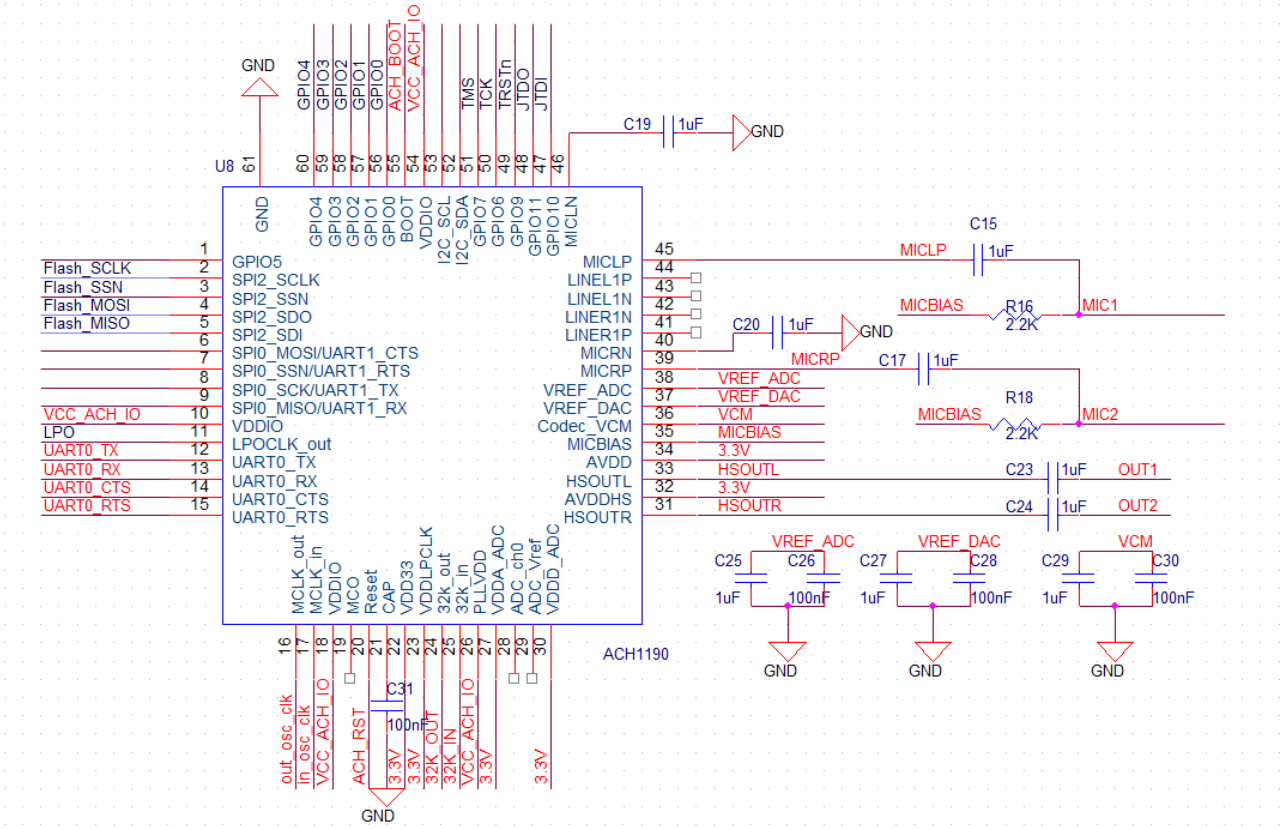
Table 10. Typical current

Core Current	HCLK Run While（1）	@1.8V No Codec	@2.5V With Codec	@3.3V With Codec	Unit
	26MHz	5.5	6.7	7	mA
	100MHz	14.2	20.6	21	mA
	240MHz	22.1	32.9	34.6	mA
I/O current	HCLK Run While（1）	@1.8V	@2.5V		mA
	26MHz	2.1	4.1		mA
	100MHz	2	3.9		mA
	240MHz	2.6	4.7		mA
Sleep	32Khz	250	400	400	uA
	26Mhz (without 32Khz)	900	1000	1000	uA

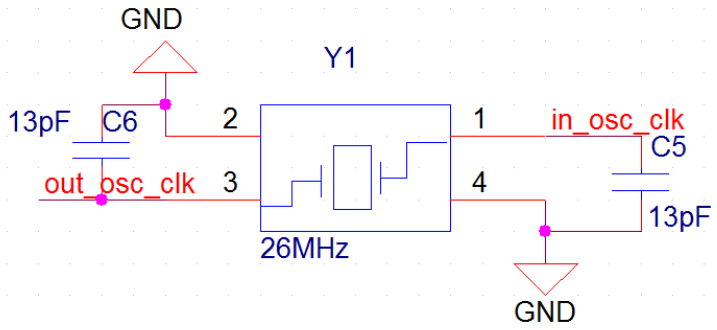
19. Hardware Reference Design Circuit

19.1. Main chip circuit

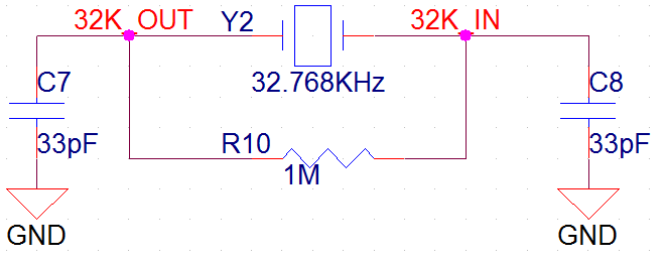
VCC_ ACH_ IO is the IO interface level voltage



19.2. 26MHz main clock

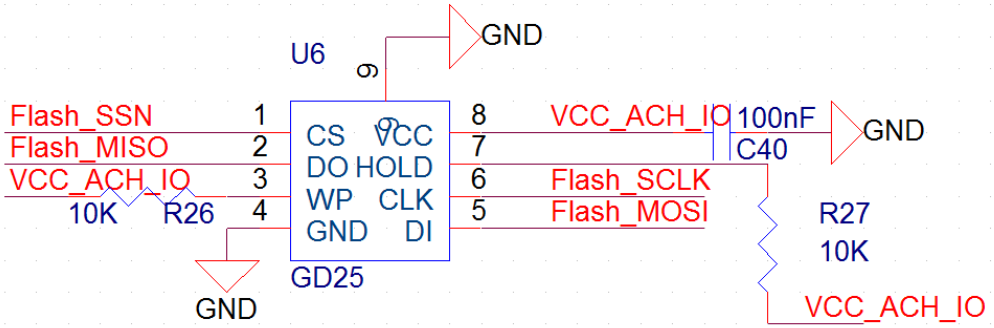


19.3. 32.768KHz Low power clock (optional)



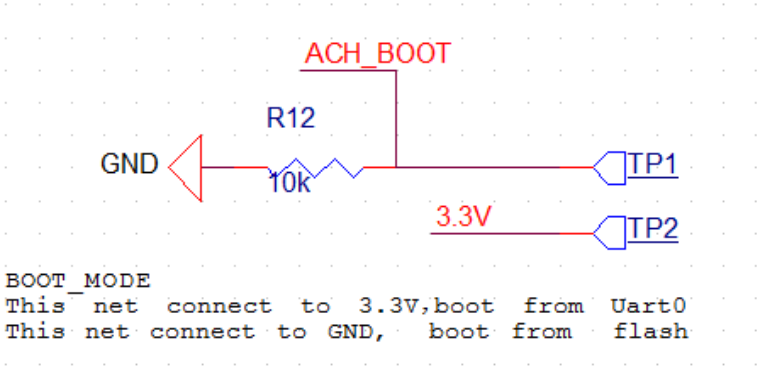
19.4. SPI2 Serial NOR Flash

Programs and data are stored in external flash and loaded from flash after reset



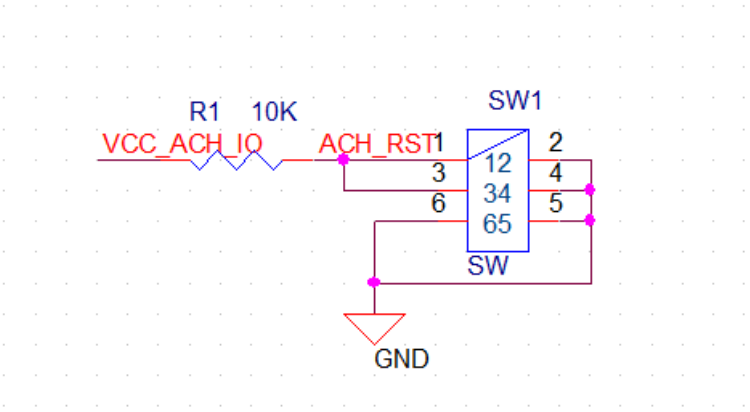
19.5. BOOT and Reset

When boot is low, startup from SPI flash
When boot is high, UART0 test mode



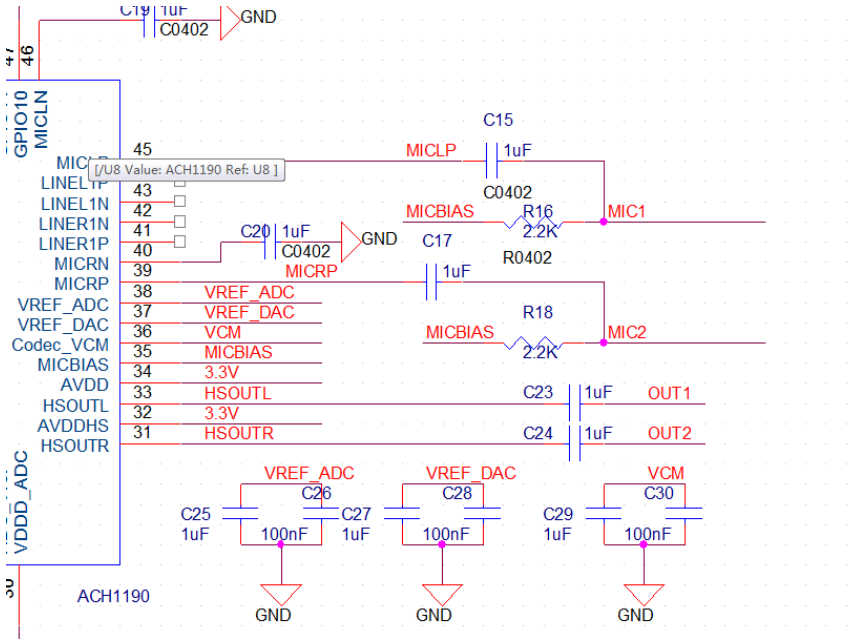
19.6. Reset

The Reset is active when the level is low



19.7. Audio

There are two audio input channels and two audio output channels. Each channel can be configured separately

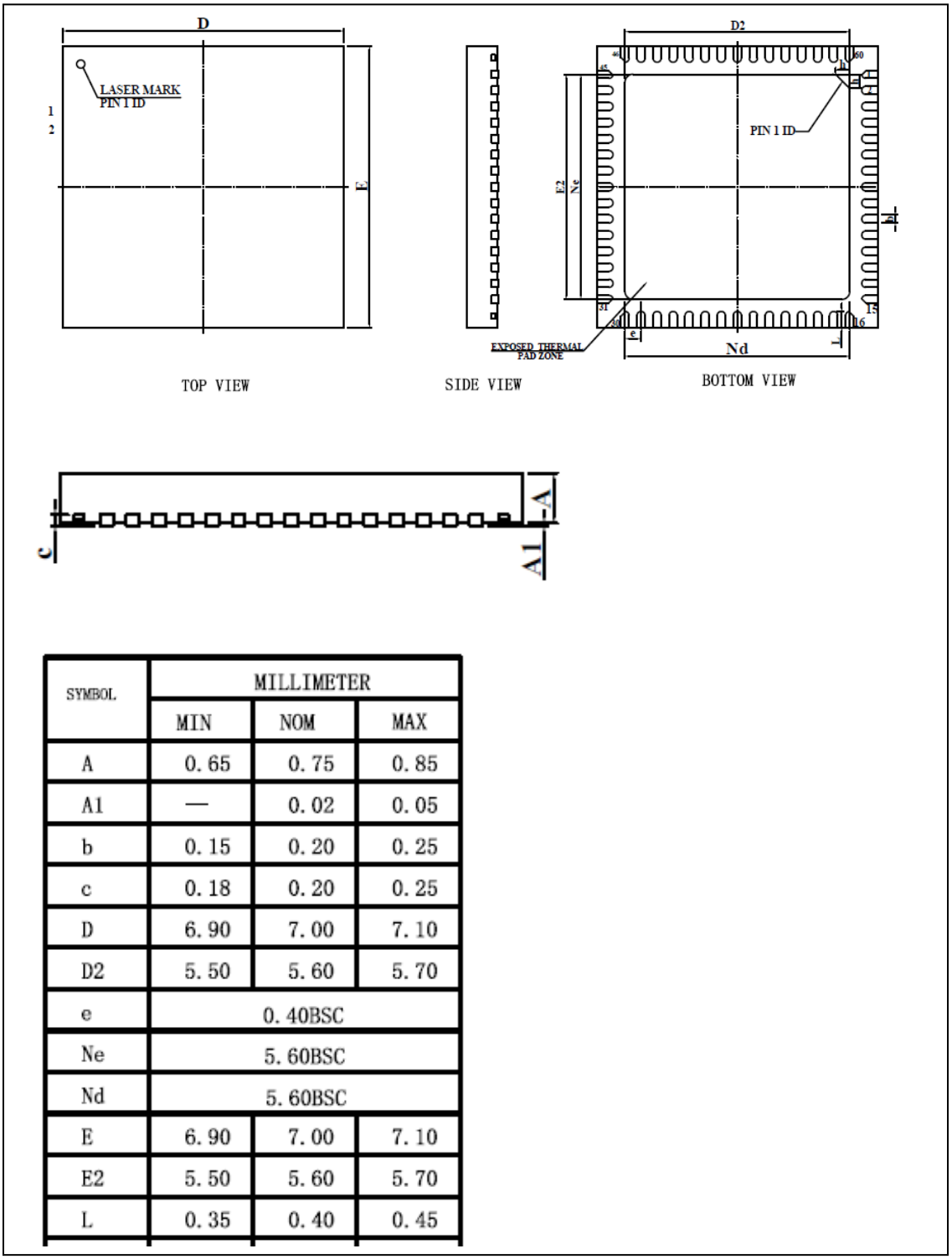


20. Ordering information

Part number	Package type	Quantity
ACH1190-Q-J	QFN60	260/Tray

21. Package mechanical data

Figure 3. QFN60-lead, 7X7mm, 0.4mm pitch, quad flat non-leaded package outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.75	0.85
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
e	0.40BSC		
Ne	5.60BSC		
Nd	5.60BSC		
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45

22.Revision history

Date	Revision	Description
8/21/2018	1.0	Preliminary version
3/18/2019	2.0	Add QFN60 package information
4/26/2019	2.1	Add features for SPI, I^2S, and CODEC
6/11/2019	2.2	Add peripheral I/O register details
6/18/2019	2.3	Update block diagram
9/16/2019	2.4	Update QFN60 pin details
9/18/2019	2.5	Change MICIP_L and MICIN_L pins for ACH1190
6/18/2020	2.6	Add low power mode section. Add ARM SCB section. Add I/O Mux control registers. Add GPIO section. Updated part number.
11/19/2020	2.7	Add timer register definitions
3/4/2021	2.8	Fixed I2S0 pin defines